THE TDA8140/43: A SELF-ADAPTING DRIVER CIRCUIT FOR HORIZONTAL TV DEFLECTION

In conventional TV horizontal deflection stages the output transistor is driven by a medium power transistor and a transformer. The disadvantage of this solution is that the drive circuit must be optimized for each application to ensure saturation of the power transistor. Moreover dissipation is higher than necessary because this type of circuit cannot supply the ideal base current. And when the chassis is turned-on or off the power transistor is stressed, compromising reliability.

The SGS TDA 8140 is a new alternative (patent pending) which solves these problems. A small power IC, it provides the optimal charge and discharge currents, adapting to different application conditions. Design is simplified and, because the base current is optimized, dissipation is reduced to a minimum.

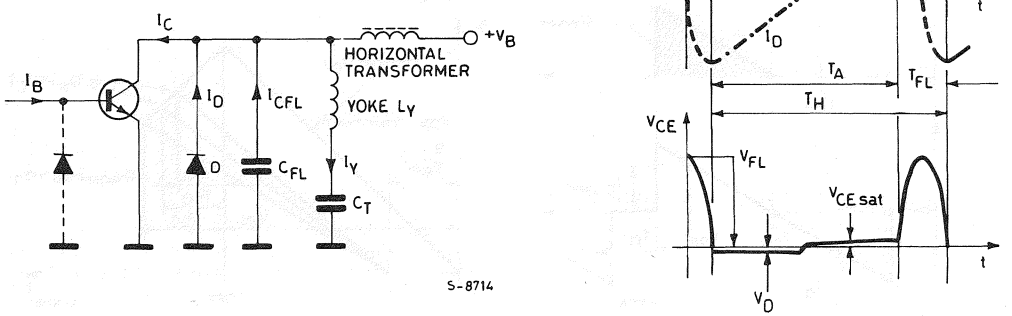
Additionally the TDA 8140 includes control and protection functions which enhance system reliability. When the chassis is turned ON or OFF, for example, the TDA 8140 ensures that the power transistor is driven correctly. And the TDA 8140 protects both itself and the external power transistor against overload conditions.

The device is available in two package: a 16-lead DIP package (type TDA 8140) and a 9-lead SIP plastic package (type TDA 8143).

PRINCIPLE OF OPERATION

A typical deflection circuit of a present chassis is shown in Fig. 1. This concept is realized by an LC resonance circuit which operates at two different frequencies, controlled by the power switch T. One complete deflection period T_H consists of the active deflection phase T_A and the flyback phase T_{FL}. During T_A, transistor T conducts for positive I_y, diode D carries the negative I_y.

Fig. 1 – Typical horizontal deflection circuit and related waveforms



Assuming a long period duration of the resonance circuit L_y and C_T, compared with T_A, the deflection current rises quasi linearly. In the flyback phase T_{FL}, the elements T and D are inactive and the current I_y has a cosinus waveshape of a much higher frequency due to the series connection of C_T and C_{FL}. The corresponding voltages are determined by a small drop V_{CEsat} and V_D during T_A respectively, the high flyback voltage during T_{FL}.

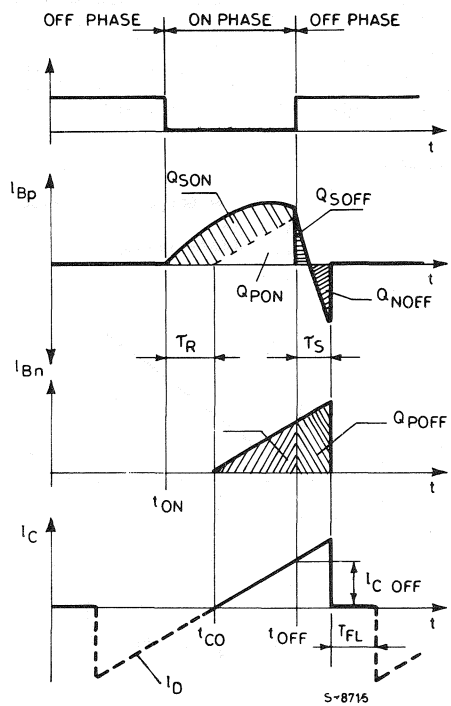
The driver circuit for the power switch must fullfill the different requirements during the ON and OFF phase.

Fig. 2 gives the typical base driving conditions for the power transistor. Normally, the transistor is activated at $t = t_{ON}$ before the zero crossover of I_C at t_{CO}. During the active phase $t > t_{CO}$, the transistor must be carefully saturated. This results in an excess base charge Q_{SON} and leads to the turn OFF delay time τ_S.

A typical deflection transistor requires $V_{CES} > 1500V$ and shows a very low current gain of $B < 5$ at about $I_C = 3.5A$.

An optimum driver circuit represents the trade off between a slow dircharge which increases the power dissipation and a fast discharge which is limited by the emitter crowding effect and the reverse second breakdown [1], [2]. The resulting storage time is achieved by a defined base current decay.

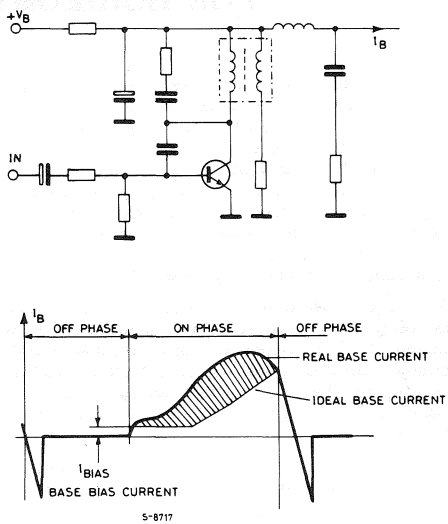
Fig. 2 - Base driving conditions



DRIVER CIRCUIT CONSIDERATIONS

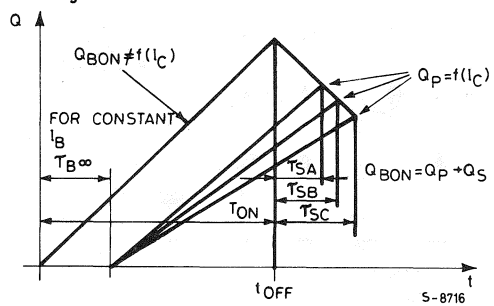
The classical driver circuit in Fig. 3 consists of a discrete transistor and a transformer. During the turn ON phase of the power transistor, the driver is switched off. The current waveform is determined by the primary RC network and is limited by a secondary series resistor. In the turn OFF phase, the negative current slope results from the transformer stray inductance or an additional discrete series coil.

Fig. 3 - Classical driver circuit and output waveform



The stability of such system is inherently fullfilled because the base charge Q_{BON} is independent of the collector current. Hence, a higher collector current results into a lower excess charge Q_S respectively storage time τ_S, corresponding to the demanded negative stability factor k_S.

Fig. 4 - Graphical explanation of the storage time τ_S

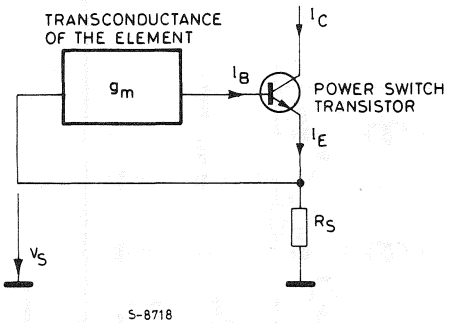


This relationship is illustrated in Fig. 4 for simplified base charges. Q_{BON} is the actual base charge and Q_p is the required base charge ensuring saturation for each of the three indicated different collector currents.

INTEGRATED DRIVER

As explained in the previous chapter, the power transistor in the deflection circuit only operates as a simple switch. Therefore, an optimum driver circuit generates the correct base current in order to guarantee saturation at each instant of time. The dynamic circuit senses the actual current in the power transistor across the emitter resistor R_S, as shown in Fig. 5 and delivers the base current.

Fig. 5 - Principle of operation of the integrated driver



$$I_B = R_S \frac{g_m}{1 - R_S\, g_m} I_C. \qquad (1)$$

The saturation condition sets the lower bound for the transconductance g_m:

$$1/R_S\,(1 + B_{MIN}) < g_m < 1/R_S, \qquad (2)$$

whereas the upper bound is given by the stability of the positive feedback loop.

A typical distribution of the current gain versus the collector current for the BU 208A transistor is shown in Fig. 6. The required base current for a minimum beta device defines the transfer characteristics of the driver, approximated by the sum of a constant and a proportional term.

The simplified circuit diagram of such integrated driver circuit (TDA 8140/43) is shown in Fig. 7. It illustrates both, the signal transfer behaviour and auxiliary protection functions.

In the normal operating mode, the control input determines two different conditions:

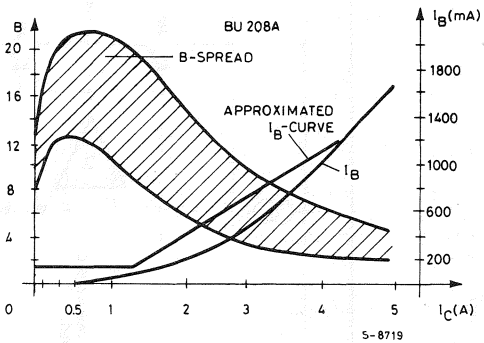
For a Low input, Q_5 is On and the element acts as a static transconductance amplifier which ensures the proper saturation of the external power transistor. A High input control signal opens Q5 and results into an output current ramp, discharging the base of the external transistor.

$$\frac{dI_B}{dt} \sim -\frac{1}{C_{EXT}}. \qquad (3)$$

Different safety functions enable the output power amplifier:

1) During the flyback phase, where the SYN DET input is High
2) For supply voltages less than 7V
3) For chip temperature higher than 160°C

Fig. 6 - Current gain and base current of the BU208



TRANSCONDUCTANCE AMPLIFIER

The main part of the element consists of a push-pull power transconductance amplifier which can deliver an output current of ± 1.5A for a wide output voltage range. This amplifier is a 3 stage design. A ground compatible input stage Q1 ÷ Q4 realizes a transconductance preamplifier with symmetrical output:

$$g_{m1} = \frac{I_1 - I_2}{V_S - V_{CEXT}} = \frac{1}{R3}. \qquad (4)$$

The output current I1, I2 is fed into the load resistors R1 = R2. Due to the feedback configuration of the further amplifiers A1 and A2, the main output current drop $I_B \cdot R5$ becomes equal to the difference voltage across R1 and R2.

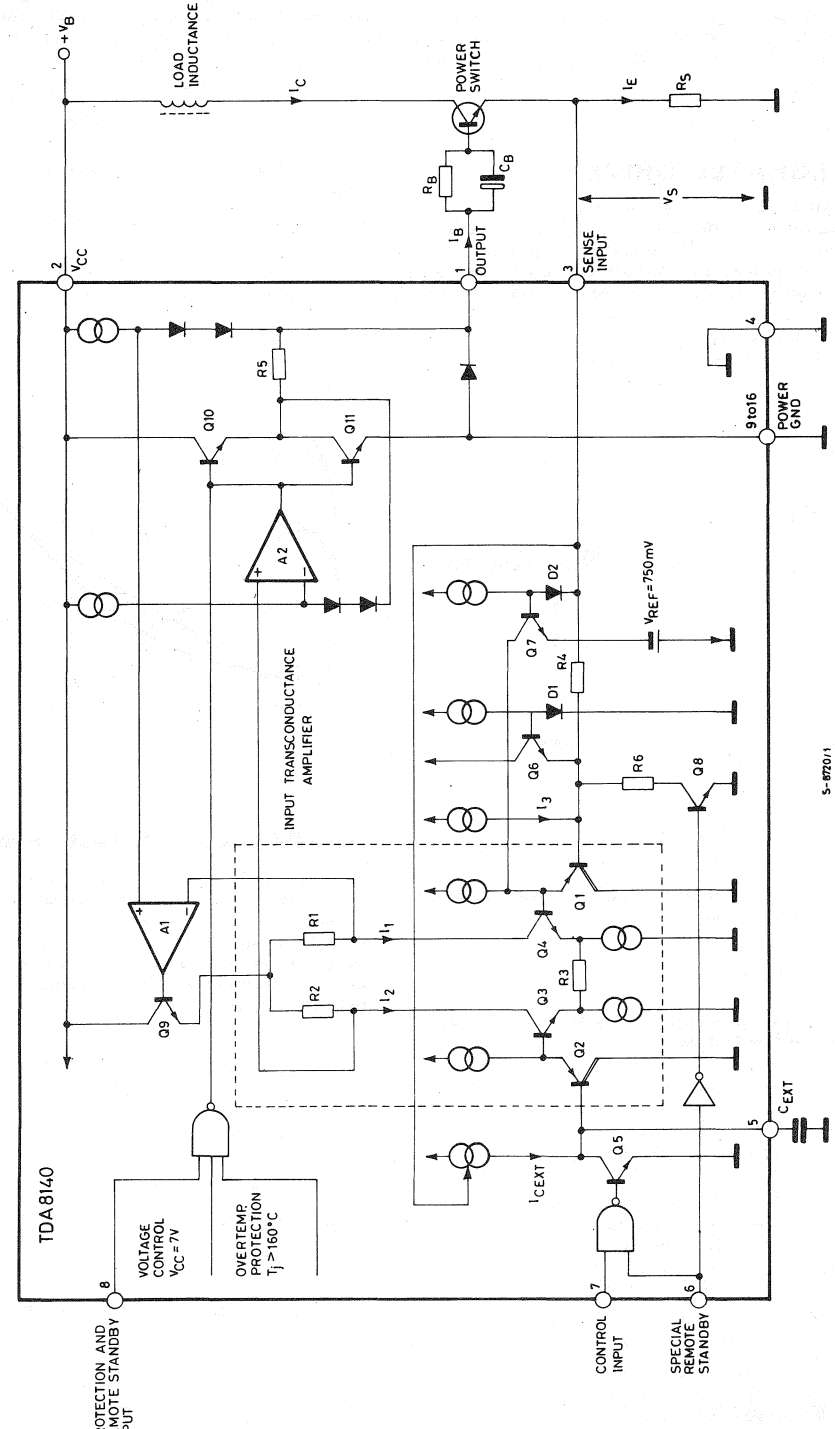
Thus, the overall transfer function g_m results into:

$$g_m = I_B/V_{IN} = 2 \cdot g_{m1}\, R1/R5, \qquad (5)$$

this gives:

$$g_m = 2 \cdot R1/R3\, R5. \qquad (6)$$

Fig. 7 – Simplified circuit diagram



The output current can be expressed as:

$$I_B = (V_S - V_{CEXT})\, 2 \cdot R1/R3\ R5. \quad (7)$$

Although the amplifiers A1 and A2 perform a positive feedback configuration, the stability of this inner loop is always ensured. As to be seen from Fig. 8, which gives a simplified structure, the additional amplifier A1 forces an inner voltage at node A, which must be identical to the output voltage at node B. Because the output power amplifier A2 has unity gain, the drop across R5 is equal to the drop across R1 + R2 which results into Eq. (7).

Considering the high output impedance of the first stage, the amplifier A1 also provides unity closed loop gain, thus the inner loop gain v_L becomes:

$$v_L = v_{A1} \cdot v_{A2} \cdot \frac{R_L + R_S}{R5 + R_L + R_S} \quad (8)$$

Careful attention is paid to the frequency compensation of A1 and A2 in order to ensure:

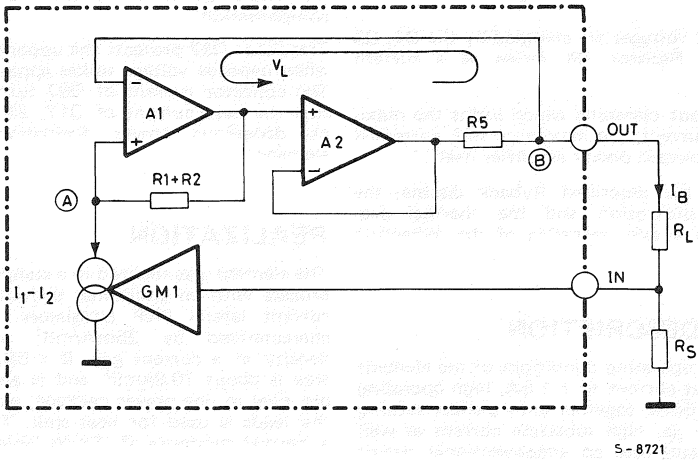
$$v_{A1} = v_{A2} \leqslant 1. \quad (9)$$

Hence, the loop gain v_L always becomes:

$$v_L < 1, \quad (10)$$

which guarantees the stability of the inner auxiliary loop v_L.

Fig. 8 - Simplified signal transfer block diagram



SYSTEM STABILITY

A controlled base current, proportional to the collector current, does not offer stability because the excess charge is reduced with a decreased collector current. Hereby, the new element would cause instability. However, such characteristic is avoided by a controller base discharge procedure. The slope of the output base current is controlled by the emitter current of the power transistor itself. As to be seen in Fig. 7, the input voltage V_S determines the charging current I_{CEXT} of C_{EXT} via a controlled current source g2.
Using:

$$I_{CEXT} = g2 \cdot V_S, \quad (11)$$

the slope dI_B/dt derived from (7), becomes:

$$\frac{dI_B}{dt} = -\frac{2 \cdot R1}{R3\ R5} \frac{dV_{CEXT}}{dt} \quad (12)$$

which results into:

$$\frac{dI_B}{dt} = -\frac{2 \cdot R1}{R3\ R5} \frac{g2 \cdot V_S}{C_{EXT}} \quad (13)$$

A high collector current of the power transistor therefore generates a fast discharge combined with a small storage time and vice versa; consequently, the system stability is obtained.

During the turn OFF phase, V_S is quasi constant because the collector current is still increasing, whereby the base current is reduced as described.

AUXILIARY FUNCTIONS

In order to start the regenerative loop together with the power transistor, the element delivers a constant current of 150mA at the output. This proportion is independent of the input voltage and is derived from the constant current source I_3. The current I_3 provides a 70mV drop across R4 as a prebias of Q1.

In the standby mode, resistor R6 is activated by the saturated transistor Q8. Both, the transconductance and the output DC current are now reduced by a factor of 3.

The operating range of the element is fixed by an input limiting circuit. For input voltages higher than 750mV, D2 activates Q7 which limits the base voltage of Q4. Therefore, the maximum output current is limited to:

$$I_{BMAX} = \frac{750mV}{R_S} \qquad (14)$$

Negative input voltages are clamped by the D1, Q6 configuration. Resistor R4 serves as a current limitation.

Beside this input clamping which limits the maximum source current, the maximum sink current is limited in the output power amplifier itself.

Furthermore, the described flyback disable, the undervoltage protection and the thermal protection ensure a safe operating of the deflection system.

CIRCUIT DESCRIPTION

Some extreme operating conditions of the element like high output current of ± 1.5A, high operating frequency > 15kHz together with a short settling time of a few μs, high substrate current as well as low drift result into an unconventional circuit design and require a careful layout.

OUTPUT POWER AMPLIFIER

The circuit diagram of the output power amplifier is given in Fig. 9. Transistors Q12, Q13, Q25, Q26, Q63 and Q16 realizd a single pole amplifier which is followed by a push-pull output buffer. The upper half is built by the emitter follower Q22 and the output darlington Q17, Q21. The maximum output voltage as a current source is given by $V_{CC} - V_{BE17} - V_{BE21} - V_{CE5}$ -; the minimum results from the saturation of Q64.

The lower half of the output stage consists of Q36, Q48 and Q66 as active element, where Q41, Q43 and Q34 serve as biasing structures.

The minimum output voltage in the current sink mode is only limited by the saturation voltage of Q66 which is less than 1.2V at 1.5A output current. A low drop current limitation at 2.5A is included in the emitter of Q66 which senses the drop across a 60mΩ metal resistor.

The fast settling of this output amplifier requires a quiescent current of about 10mA. With respect to the temperature stability of this current, the current densities of the related elements fullfill the cancellation condition:

$$\frac{I_{17}}{A17} \cdot \frac{I_{21}}{A21} \cdot \frac{I_{48}}{A48} \circ \frac{I_{36}}{A36} = \qquad (15)$$

$$= \frac{I_{41}}{A41} \circ \frac{I_{43}}{A43} \circ \frac{I_{22}}{A22} \cdot \frac{I_{34}}{A34}$$

A 350mΩ emitter diffused resistor R37 realizes the output current sense element. Using a double diode level shift - Q37/38 and Q40/42 - the drop voltage can be applied to a standard NPN differential amplifier. Thus slow input PNP elements can be avoided. Additionally, a clamping circuit Q14, Q23 prevents the forward polarization from the diode C4 which is used for the frequency compensation.

Transistor Q87 protects the upper power transistor when negative voltage spikes appear at the output. The collector current of Q87 turns Q5 off which cuts the base current of Q17, 21. By this means, no dangerous power dissipation imperils the element.

REALIZATION

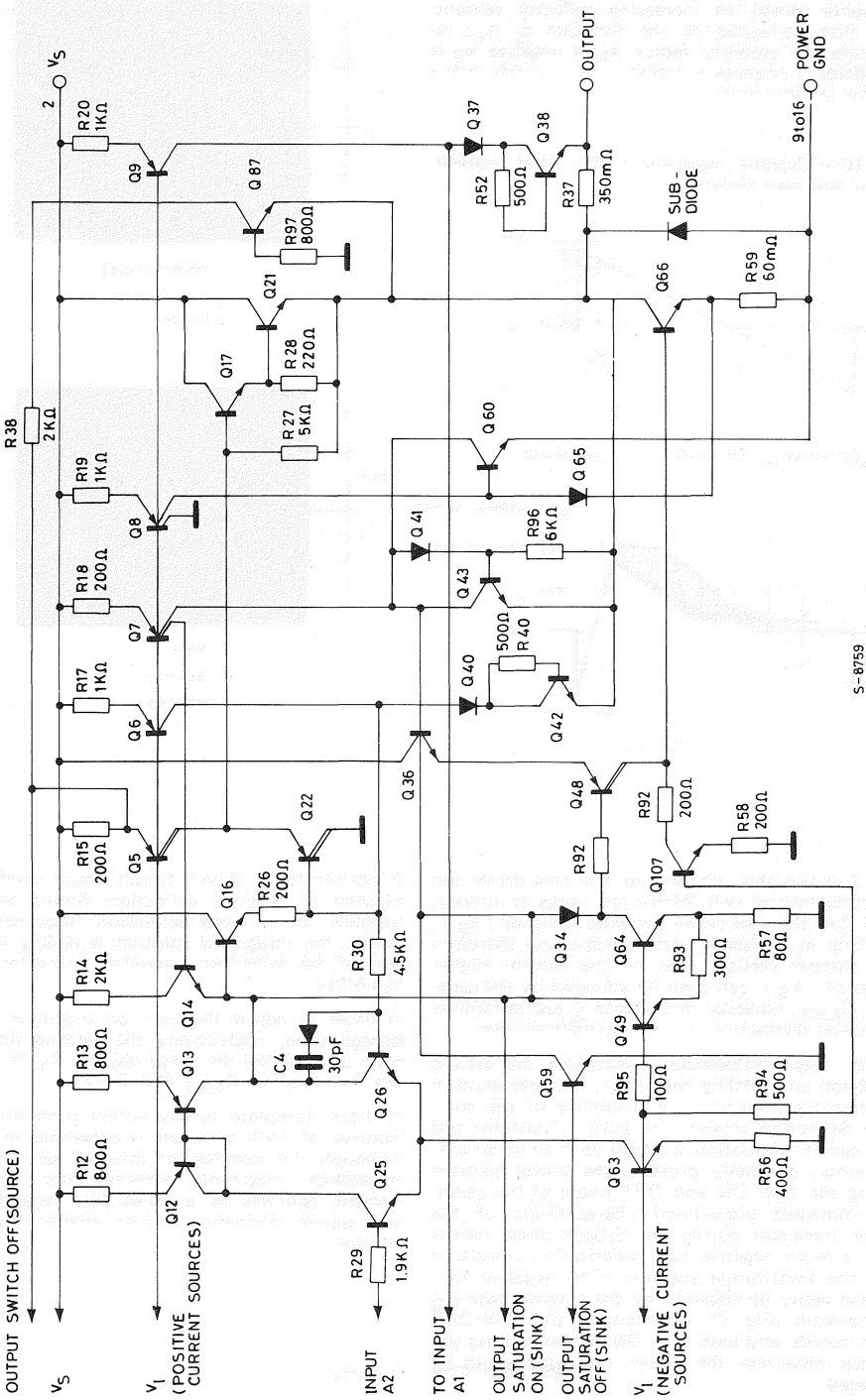
The element was realized in a standard 18V V_{BCEO}, process with an additional diffusion step for high current lateral PNP transistors. The process is characterized by 25mA/mil^2 emitter current density at a current gain $B = 5B_{MAX}$. The chip area is about 10.8kmil^2 and is assembled in a 16 pin dual in line power package, where one side of the leads is used for heat sink. This package has a thermal resistance of 15K/W (chip to leads).

EXPERIMENTAL RESULTS AND COMPARISON TO THE DISCRETE DRIVER

The performance of the TDA 8140/43 integrated driver has been investigated both theoretically and experimentally. The collector current of the power transistor, together with rhe related base current for the ideal case, the conventional driver and the new one is presented in Fig. 10. A significant difference is clearly visible in the heatched area, representing the excess base charge. The new driver nearly the classical driver provides only a rough approximation of this objective function due to the limit number of components.

The practical results confirm this described difference. Fig. 11 shows the measured collector and base currents for the conventional driver (top) and for the new driver (bottom), applied in the same chassis.

Fig. 9 – Complete output power stage



As discussed above, the stability of the deflection requires a decreasing storage time τ_S of the power transistor versus an increasing collector current. The first derivative of the function τ_S (I_C) represents the stability factor k_S; a negative k_S is mandatory, whereas a higher $|k_S|$ yields into a shorter settling time.

Fig. 10 - Current waveforms for ideal conventional and new circuit

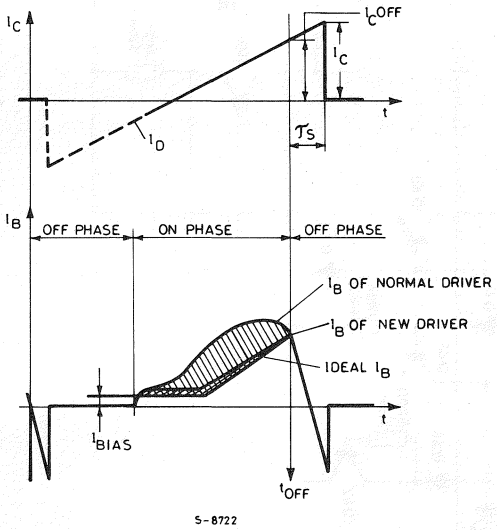


Fig. 11 - Measured collector and base currents

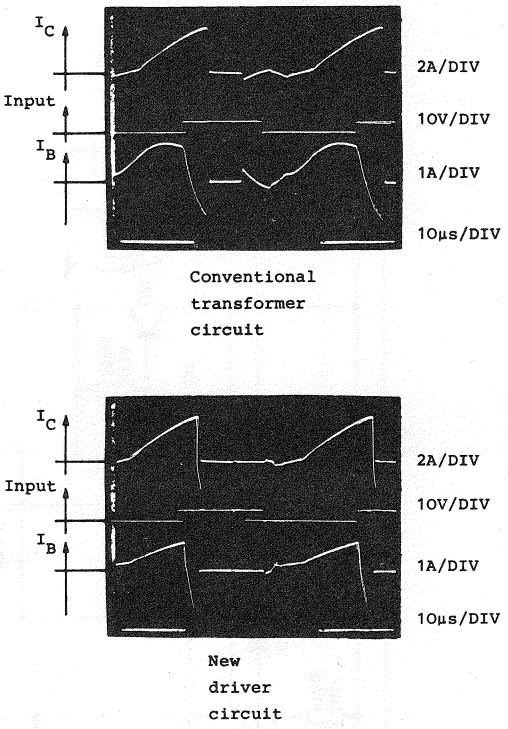


Fig. 2 shows this relation for the new driver and the conventional one. Within the range of interest, $I_C \approx 3A$, the new driver provides a higher $|k_S|$, resulting in a shorter settling time and therefore into sharper vertical lines on the screen. Higher values of $|k_S|$ can even be adjusted by the capacitor C_{EXT}, however, the chosen τ_S just minimizes the power dissipation in the external transistor.

Beside these differences, concerning the driving condition and settling behaviour, the now solution significantly improves the reliability of the complete deflection circuit. The built in collector and base current limitation together with an undervoltage sense, optimally protects the power element during the turn ON and OFF phase of the cassis. An improved breakdown characteristic of the power transistor during the flyback phase results from a more negative base polarization compared with the transformer solution. This negative voltage can easily be adjusted by the external base R_B C_B network (Fig. 7). Additionally, the SYN DET input avoids any base turn ON current during the flyback otherwise the power transistor could be damaged.

A conventional driver circuit must carefully be adapted to a given deflection circuit and only operates for a fixed deflection frequency. Contrarily, the integrated solution is widely independent of the deflection frequency and offers a high flexibility.

In order to adjust the turn on overdrive and the storage time, respectively the settling time, one must only define the sense resistor R_S (0.1-0.3Ω) and the capacitor C_{EXT} (0.5-2nF).

A more complete survey which summarizes the features of noth concepts is presented in Tab 1. Although the transformer solution can realize an impedance matching, whereas the integrated element operates as a series pass regulator, the total power dissipation is even smaller in the new solution.

Fig. 12 - Illustration of the stability factor K_s

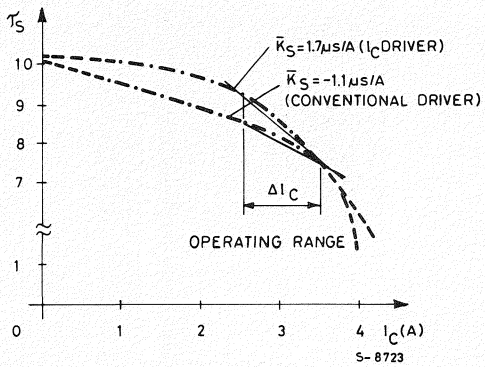


TABLE 1 - Table of key performance summary

Characteristics	TDA 8140 TDA 8143	Conventional Driver
RELIABILITY		
I_C limitation	yes	no
I_B limitation	yes	yes
Undervoltage sense	yes	no
Flyback disable	yes	no
Neg. V_{BE} (Turn OFF)	-2V to -6V	-2V
DEFLECTION FREQUENCY	independent	fixed design
APPLICATION ADAPTATION	one R, one C	several R, C transformer
SETTLING TIME	short (adjustable)	fixed
COMPONENTS	5 to 7	10 to 15
TOT. POWER DISS. (30AX, f_C = 3.2A)	2.5W	3.2W